

**Amendments to the Claims**

1. *(Original)* A nanowire with a first, a second, and a third region in an axial arrangement,

wherein the second region adjoins the first and the third regions and has a length of less than 100 nm in axial direction, and

wherein the second region has a greater diameter than the first and the third region, in which first and third regions quantization effects take place.

2. *(Original)* A nanowire as claimed in claim 1, characterized in that the second region has a length in axial direction of less than 20 nm.

3. *(Currently Amended)* A nanowire as claimed in claim 1, ~~claim 1 or 2~~, characterized in that the first and the third region have an average diameter in radial direction of at most 10 nm.

4. *(Original)* A nanowire as claimed in claim 3, characterized in that the second region has a maximum diameter of 50 nm.

5. *(Original)* A nanowire as claimed in claim 1, characterized in that the first region is n-type doped and the second region is p-type doped.

6. *(Original)* A nanowire as claimed in claim 1, characterized in that a fourth and a fifth region are present, which fourth region is enclosed in axial direction by the third and the fifth region and in axial direction has a length of less than 100 nm, and which fourth region is structurally different from the third and fifth regions in that it has a smaller bandgap.

7. *(Currently Amended)* An electronic device provided with a first and a second electrode which are interconnected by means of at least one nanowire, characterized in that the nanowire as claimed in claim 1 is present. ~~—in any one of the claims 1 to 6 is present.~~

8. (*Currently Amended*) An electronic device as claimed in claim 7, characterized in that the nanowire of claim 6 is present, and in that a first and a second gate electrode are present, wherein a perpendicular protection of the first gate electrode on the nanowire overlaps the second region and a perpendicular projection of the second gate electrode on the nanowire overlaps the fourth region.

9. (*Currently Amended*) A method of manufacturing nanowires as claimed in claim 1, by means of catalytic growth, wherein the second region is grown at a higher temperature than the first and the third region.

10. (*Currently Amended*) A method as claimed in claim 9, characterized in that the method comprises the steps of:

- [[ - ]] growing the first regions of the nanowires at a first growing temperature;
- [[ - ]] growing the second regions of the nanowires at a second growing temperature which is higher than the first growing temperature; and
- [[ - ]] growing the third regions of the nanowires at a third growing temperature which is lower than the second growing temperature.

11. (*Currently Amended*) A method of manufacturing nanowires as claimed in claim 1, ~~claimed in any one of the claims 1 to 6~~, comprising the steps of:

providing a patterned etching mask at a surface of a semiconductor substrate; and  
etching the semiconductor substrate so as to form the nanowires in a direction substantially perpendicular to the surface, during which the etching rate is reduced while the second region of greater diameter is being formed.

12. (*Original*) A method as claimed in claim 11, wherein the nanowires are removed from the semiconductor substrate.

13. (*Currently Amended*) A dispersion of nanowires as claimed in claim 1, ~~any one of the claims 1 to 6~~ in a dispersing agent.